

LOW VOLTAGE TRANSIENT VOLTAGE SUPPRESSOR AND METHOD OF
MAKING

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Abstract of the Disclosure

A method of providing a Transient Voltage Suppression (TVS) device is described utilizing a Metal Oxide Semiconductor (MOS) structure and an Insulated Gate Bipolar Transistor (IGBT) structure. The MOS based TVS devices offer reduced leakage current with reduced clamp voltages between 0.5 and 5 volts. Trench MOS based TVS device (72) provides an enhanced gain operation, while device (88) provides a top side drain contact. The high gain MOS based TVS devices provide increased control over clamp voltage variation.